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A Review: Low power and High Speed CNTFET based SRAM Cell for Data Centers

Ranjeet Singh Chauhan[1], Rajesh Mehra[2]

[1]Department of ECE, NITTTR, Chandigarh, India
[2]Department of CDC, NITTTR, Chandigarh, India

ABSTRACT

In present scenario cloud computing and virtual data centers become an integral part of day to day life. As the number of internet users increases exponentially and online streaming increasesdrastically in recent years the need of virtual data centers increases. These virtual data centers consist of processors, memory (i.e. Static Random Access Memory), RAM (Random Access Memory) and power supply. The power consumed by these data centers is almost 1.5% to 2% of total electricity consumptions which is huge amount. To reduce this power consumption, area requirement and increase speed of virtual data centers it is necessary to further scale the CMOS circuit. In this paper existing work is reviewed and seen that the various other devices like FINFET, TFET and CNTFET are tried by the researchers but CNTFET gives the better gate control and low leakage current. So, various model of Carbone Nano Tube Field Effect Transistor (CNTFET) are reviewed for the application of Static Random Access Memory (SRAM) which is used for Virtual data center in Cloud Computing. Different Model are explained and discussed for the better speed, and to reduce power and area requirement.

Keywords:- ***CNTFET, SRAM, Data Centers, Cloud Computing, VLSI.***

I. INTRODUCTION

Recent Studies shows that power consumption, area requirement and data transmission speed are the main constraint of research in Static Random Access Memory. Virtual data centers which is used in cloud computing require these SRAMs but with increase of online users power requirement, area requirement and data transmission speed become a big problem for industry.

Cloud computing is need of time and it has become one of premier technology of modern era. Almost every premier institutions, important industries and cooperate offices uses cloud computing to increase productivity and reduce operational cost. Although some them is hesitating in join cloud computing due to security reasons. As research increases all the problem and security concerns may short out. Generally hypervisors are used to manage virtual machines for sever consolidation. This manage the machines virtually reduces the physical demand of the operation. It can be managed by service providers who offer Software as a Service (SaaS) Platform as a service (PaaS) and Infrastructure as a Service (IaaS). These techniques are implemented in different types according to demand and need of users as

- Private Cloud: These types of models are specially implemented for the individual organization for specific purpose. These types model deployment is costly because it is used by single organization.
- Public Cloud: This is a shared model which is shared by different organization simultaneously. As it is shared by multiple companies so it require mega infrastructure to provide services to many companies efficiently. Due to sharing of infrastructure and services this model is cheaper than private cloud model
- Hybrid Cloud: It is combination of public and private model. It consist of both types to deployment model as it used for lease for public and also used for organizations in house work.
- Community Cloud: This types of model used by specific community and organization to provided special sevices.

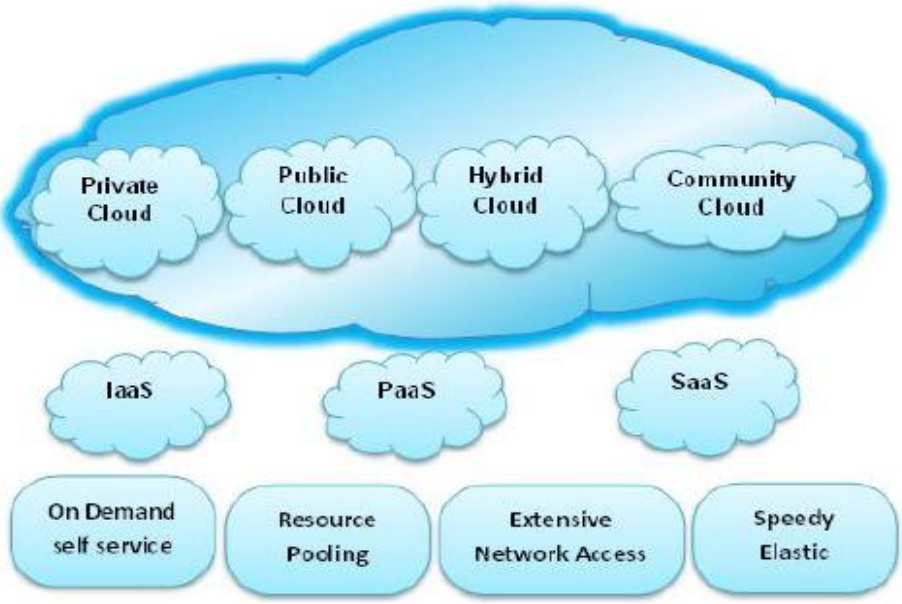

Fig.1.Cloud Deployment & Service Model

Virtual data centers are mainly used in Infrastructure as a service (IaaS) in which on demand service is provided as network services, computing services. Premises of these data centers allow the organization install new services without changing its hardware. These data centers make organization cost effective and efficient and provide the facility to avoid purchasing of new hardware. One of the greatest benefits of these virtual data centers is that it provides small organization to access all these services without having setup of their own center. They can use the services just paying for the service that they use. These data centers use Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM) to store the data.

A low power high speed SRAM is required by almost every VLSI circuit. Especially Virtual Data Centers require low power, high speed SRAM which require minimum area. As technology advances number of transistors on single chip is increases due to this integrated circuit require more power because power dissipation increases and also area requirement increases. A SRAM circuit is basically a cross coupled bi-stable invertor cell. The invertor are connected to each other in cross coupled manner as shown is figure

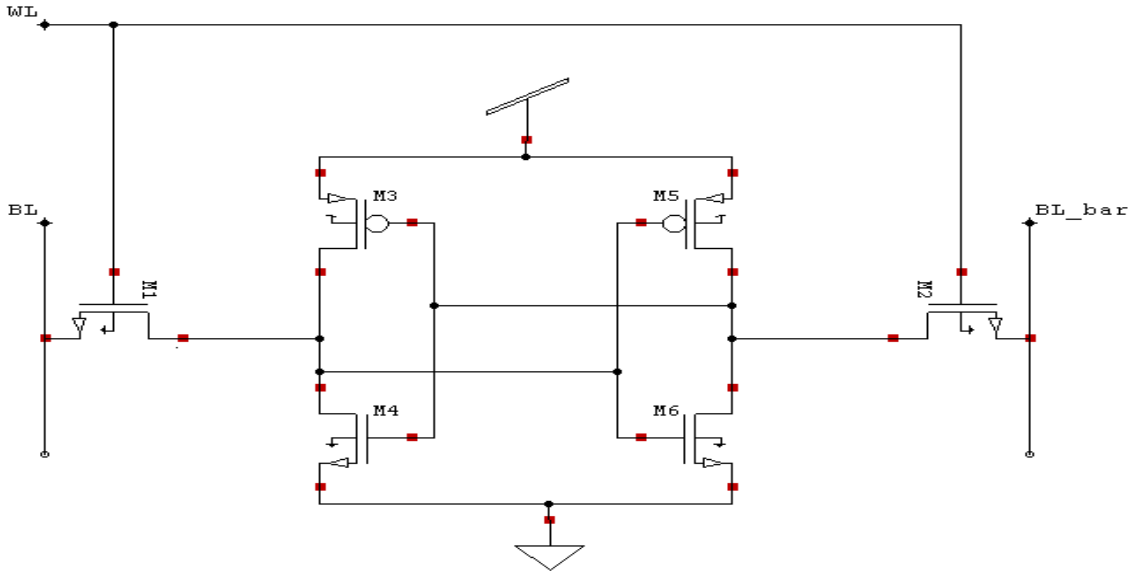

Fig.2. Basic SRAM cell [9]

SRAM which are available in market is generally madeup of CMOS ciruit where invertors are cross coupled .Scaling of CMOS circuit below 10 nm is facing problem because gate loses its control. The other option is to control the leakage current is change the geometry or material. As further scaling reduces the t_{ox}(Oxide thickness) if $thet_{ox}$ reduces to nm device leakage current is very high. If the t_{ox}doesn't shrink with material gate looses its controls. So there are two option are their

- Change the material
- Change the geometry

Actually the t_{ox}doesn't matter, capacitance matters which depends on k as Cox=εoK(A/tox) . So change the material from Sio2 (3.9) to Hfo2 (16). But it is does not provide satisfactory results. When go for change the geometry there are several geometry available one of them is FintFET and CNTFET. The FinFET provides better controls over gate as wrapping gate around the channel. The thinner the body WFIN smaller the device. As Shown in fig

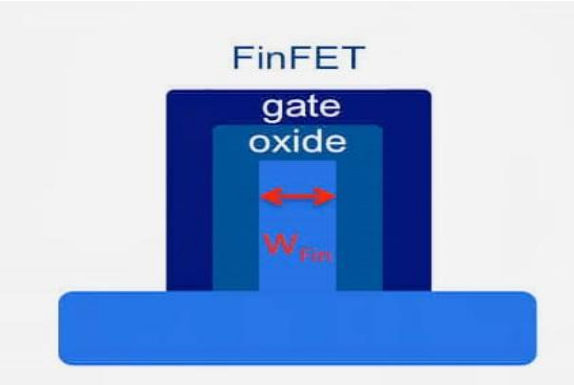

Fig.3. Basic Structure of FinFET

But if gate is wrapped from all the side it gives better result as in case of CNTFET. In Carbon Nano Tube Field Effect Transistors (CNTFET) there is no degradation down to 9 nm channel. CNTFET 1 D confinement make scattering rare and it rise to ballistic transport. CNTFET has better control during off state and has speed in terahertz. CNTFET has high k compatibility, stability and low power consumption. CNTFET structure shown in below fig

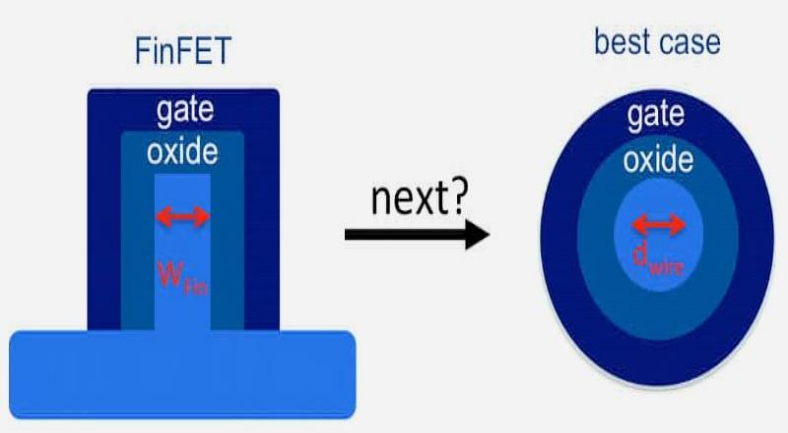

Fig.4. CNTFET Basic Structure

II. LITERATURE REVIEW

Shitaljoshi et al. in [1] discussed comparative study of 6T, 7T, 8T, 9T, 10T CNTFET based SRAM as CMOS technology faces problem of scaling below 10nm and also has poor leakage current control capacity. SRAM due to its unique feature to retain data is one of the most popular memory elements used in most of the digital circuit. Author has concluded that

CNTFET based SRAM is better than CMOS SRAM. Pejman Hosseinium et al. in [2] reported that CNTFET emerged as an alternative material to silicon for high performance, high stability and low power SRAM computers and many portable devices. In this paper designed CNTFET SRAM is better than CMOS and FinFET based SRAM. Proposed SRAM cell's is to reduce about 48% dynamic power consumption and SNM is widened up to 56% compared to the conventional CMOS SRAM structure at the expense of 2% leakage power and 3% write delay increase.

Naagesh.S.Bhat et al. in [3] reported SRAM cell is designed using Carbon Nano Tube FET at 32 nm technologies to reduce write-power dissipation and to reduce read delay. The circuit is designed and simulated HSPICE using Stand ford CNTFET model at 6T cell. Read SNM of 8T, 9T , 10T cells are about 50% higher than the 6T cell. The ease of writing ability on the 10T SRAM cell is greater than the other. It shows 60% improvement in their read SNM and 13% reduction in standard deviation. Mohitaet.al., in [4] performed comparative study of CNTFET based 6T SRAM and CMOS 6T based on180nm and 45nm. All the simulations are carried out in to cover the different aspect of SRAM cell stability analysis using butterfly curve and N-curve method. These different technologies were consider and a comparative analytical performance overview has been presented and concluded noise margin enhanced by CNTFET based SRAM

Rajendra Prasad Somineni et al. in [5] discussed different CNTFET based SRAM circuit level leakage power reduction techniques using sleep transistor, Forced stack, Data-Retention sleep transistor and Stacked sleep and concluded that stacked sleep CNTFET SRAM cell is best in terms of leakage power saving with state saving capability. Sheng Lin et.al., in [6] described CNTFETs in 6T SRAM design as threshold voltage of CNTFET cab be controlled easily by changing the chirality vector (i.e diameter) of CNTs. As the result concluded that dual-diameter CNTFET SRAM is better in stability , power and delay and also has lower sensitivity to PVT variations.

Bhubon Chandra et al. in [7] explained that to reduce short channel effects(SCEs), it is important to select a proper dielectric. After perform comparative study between Si, InAs and CNT FET author concluded CNT has better SCEs

II. INFERENCES DRAWN OUT OF LITERATURE SURVEY

A suitable optimization of Static Random Access Memory (SRAM) cell architecture is important in designing of VLSI Integrated circuits and, in specific, for factors like less delay, smaller chip area and lower power dissipation. SRAM cells are most effective components in applications like ADCs, DACs,Cache memory and wireless devices. The SRAM cell draws most power and occupies major area in these applications, thus it is important to control these parameters. Low power and smaller chip area have become an important area of concern in today's emerging era of electronic designs. To save the circuit designs from power dissipation and also to control the power consumption at the input is the major concern of researchers in order to improve the efficiency of electronic gadgets or electronics circuitries. Therefore various methodologies have been applied for designing of smaller chip area circuitries and systems. It has been observed form the survey discussed above the chip area has been reduced by using GDI, TG and MTL technique and thus control the power consumption and dissipation. Also, the systems are improved in speed and delay by using GDI, TG and MTL techniques.
Delay is also one of the important factors in sensitive applications like Video Processor, which could lower the performance of the system despite having any number of improvements in the design factors. Thus to improve the performance in delay the researchers have used optimum value of compensation value and using GDI model modifications.

IV. PROBLEM DEFINITION

CMOS technology below 10nm suffers limitation of scaling.Designing of smaller chip area is more challenging when the supply voltage is kept smaller.Most of the work in SRAM has been done for reduction of chip area, which will ultimately reduce power dissipation and lower speed effect.All designs encounter the issue of chip area design while improving the power performance factor.If the power dissipation is overcome then in that case chip area and propagation delay is affected, also, the problem of settling error arises. so there is still gap to improve the CNTFET based SRAM.In order to fill this gap the architecture should be optimized for area and delay keeping power performance factors at satisfactory levels.

CONCLUSION AND FUTURE SCOPE OF WORK

To increase the performance of virtual data centers it is necessary reduce chip area and power consumption of SRAM. CNTFET based SRAM have the capability to trade of between power, speed and area. From above discussion it is clear that CNTFET is good replacement of CMOS based SRAM. Scope of present work is mostly in the direction of chip area designing in VLSI technology. The improvement in power and noise factors decreases the scope for improved area and

speedy designs in CNTFET based SRAM. Therefore optimization of area and speed is important for application specific designs. The VLSI concept and CADENCE circuit simulator shall be used to achieve the performance improvement.

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