International Journal of All Research Education and Scientific Methods (IJARESM), ISSN: 2455-6211
Volume 8, Issue 12, December-2020, Impact Factor: 7.429, Available online at: www.ijaresm.com

Comparative Analysis of Modified CSLA Dominated by Carry Generation Logic with SQRT CSLA Adder

Y Kavya Kiran[1], K Bala Sindhuri[2], N Udaya Kumar[3]

[1]PG Student, Dept. of ECE, SRKR Engineering College, Bhimavaram, AP, India
[2]Assistant Professor, Dept. of ECE, SRKR Engineering College, Bhimavaram, AP, India
[3]Professor, Dept. of ECE, SRKR Engineering College, Bhimavaram, AP, India

----------**********----------

ABSTRACT

ACarry Select Adder (CSLA) is one of the simplest and fastest adder that performs high speed operations by using Ripple Carry Adders(RCA) and multiplexers which can be best suited for arithmetic circuits, MAC units and other digital systems. To further improve the performance in terms of area and power consumption, Modified CSLA dominated by carry generation logic is designed by using logic optimization technique. The main objective of this modified CSLAdominated by carry generation logic is to reduce Carry Propagation Delay (CPD) by employing bit slice logic along with the optimized width functional blocks.In this paper, comparative analysis for different adders such as modified CSLA dominated by carry generation logic andSQRT CLSA is done. Simulation and synthesis results are carried out usingXilinx Vivado v2017.2 software tool. The outcomes show that the modified CSLA dominated by carry generation logic by using 32-bit reduces the combination delay (ns) by 17.40%, power consumption (W) by 19.33% and LUT's by 60.52% compared to SQRT CSLA.

Keywords: Modified CSLA dominated by carry generation logic, SQRT CSLA.

I. INTRODUCTION

Power efficient circuit designs expanded theirimportancein digital technologydue to the demand of portable devices. Day by day, itbecomes a challenging issue for many researchers to perform fastadditionsand to reduce the power consumption of adders. In the present scenario, many research works have been done to improve the performance of these parameters. Various studies have reported on different methodologies to reduce the CPD in RCA, including the high speed and energy efficient Carry Select Adder (CSLA) [1-2], Carry Save Adder (CSA) [3–6], Carry Look-Ahead Adder (CLAA)[7-9] and Carry Skip Adder (CSKA) [10].One of the fastest adders which implements in a step by step manner to reduce power consumption by adopting universal gates in the design of adder is CSLA dominated by carry generation logic. It suits for portable and area efficient applications [1]. The design of carry select adder is presented in section II, A Modified CSLA dominated by carry generation logic is presented in section III, Simulation and synthesis results are explained in section IV, and Conclusionis explained in section V are discussed below.

II. DESIGN OF REGULAR SQRT CSLA

The VLSI architecture of SQRT CSLA is designed by B RAM KUMAR et.al. [2] to improve speed which is accomplished by evaluating sum and carry in advance by assuming input carry is equal to 'zero' and input carry is equal to 'one' for the partitioned groups. Selection of sum output and carry output is taken care by multiplexer unit in each and every group except the first group as shown in Fig.1.The grouping is done in an increasing fashion such that the speed of the adder is improved.

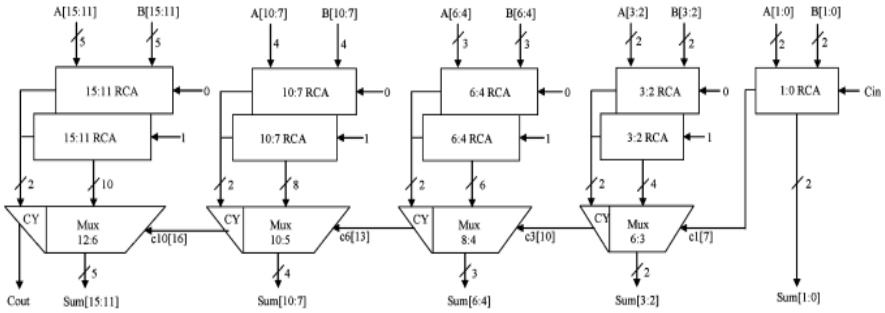


Fig.1: Regular SQRT CSLA

III. MODIFIED CARRY SELECT ADDER (CSLA) DOMINATED BY CARRY GENERATION LOGIC

The design of modified CSLA dominated by carry generation logic consists of ModifiedPrimary Carry Unit (MPCU) i.e., by using modified OR-gate, Wave Carry Unit (WCU0-WCU1), Final Selection Unit (FSC) to improve speed and to decrease number of LUT's and power consumption. In MPCU block of modified CSLA dominated by carry generation logic, a modified OR-gate using multiplexer is used instead of OR gate. The structure of modified CSLA is shown in Fig.2.

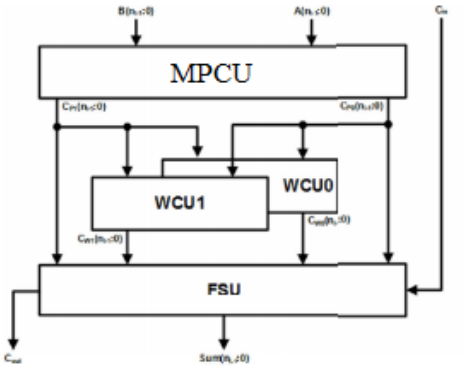


Fig.2: Structure of Modified CSLA

The designed architecture of dominated CSLA dominated by carry generation logic is shownin Fig.3 and it involves four blocks, namely:Primary carry Unit, Wave carry Unit, Final Selection Unit and Bit Slice Block of designed CSLA[1]. The PCU is modified by employing modified OR gate as shown in Fig.4.The inputs of modifiedOR-gate using multiplexer are '0' and '1' and 'Y' is the output. Here, 'A' is taken as selection line.Here OR operation is done. If A=0 then Y=B. if A=1 then Y=1. The block diagram of OR-gate using multiplexer is shown in Fig.4. The simulation and synthesis results are obtained by using Vivado 2017.3 software tool.

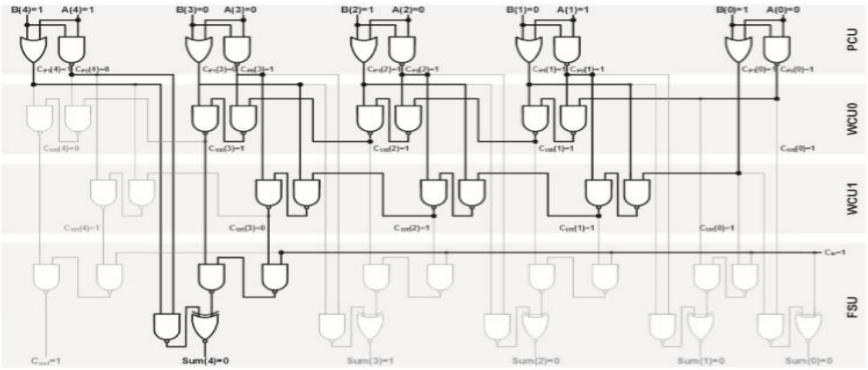


Fig.3: Modified CSLA dominated by carry generation logic

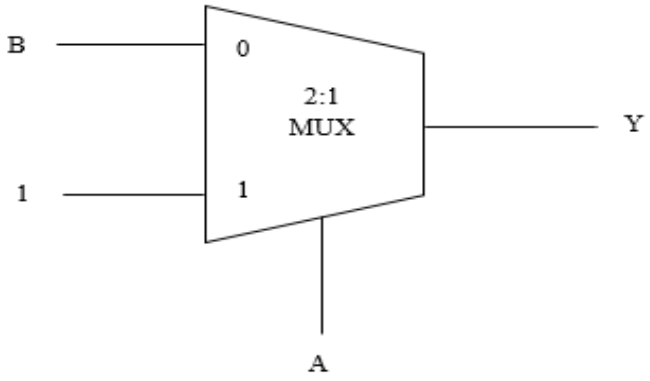


Fig.4: Block diagram ofOR-gate using multiplexer

IV. SIMULATION AND SYNTHESIS RESULTS

The simulation and synthesis results for modified OR -gate,16-bit and 32-bit adders are discussed below. The obtained simulation results for modified OR-gate using multiplexerfor different combinations is shown in Fig.5. Simulation results for 16-bit and 32-bitfor modified CSLA dominated by carry generation logic is shown in Fig.6, and Fig.7. Simulation results for 16-bit and 32-bit SQRT CSLA architectures isshown in Fig.8, and Fig.9.

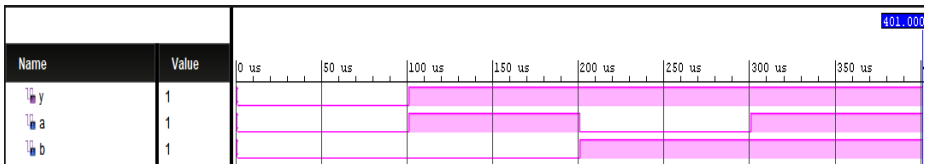


Fig.5: Simulation result for modified OR-gate using multiplexer

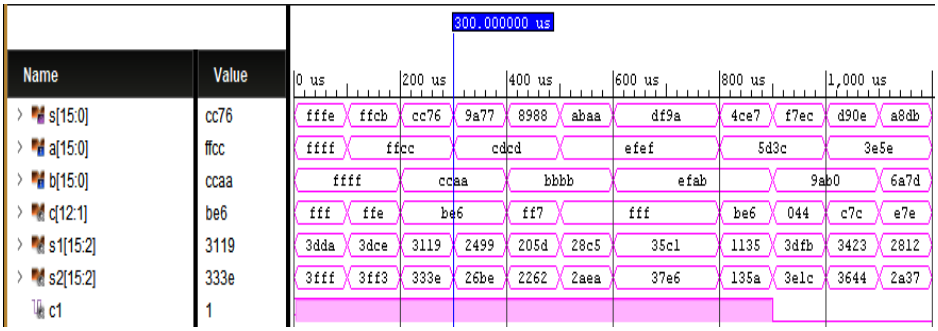


Fig.6: Simulation result for 16-bitmodified CSLA dominated by carry generation logic

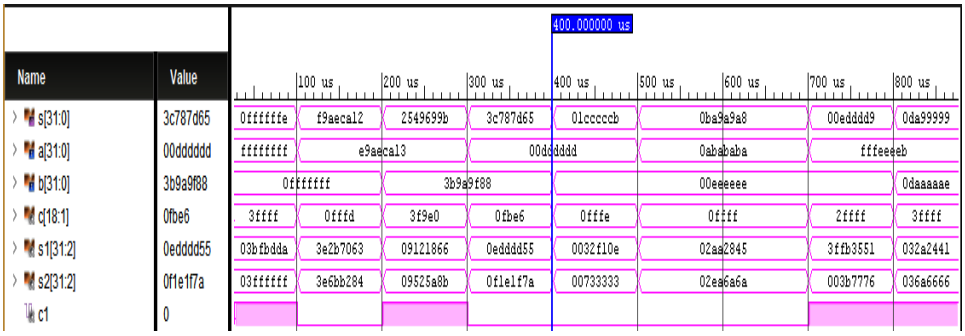


Fig.7: Simulation result for 32-bitmodified CSLA dominated by carry generation logic

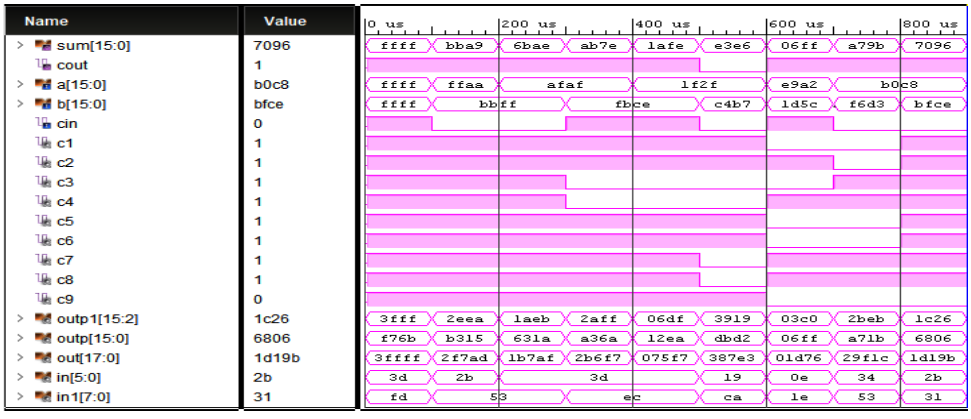


Fig.8: Simulation result of 16-bit SQRT CSLA

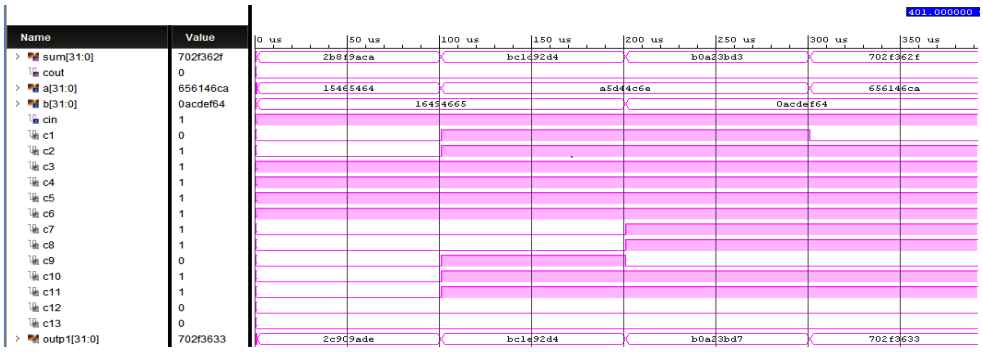


Fig.9: Simulation result of 32-bit SQRT CSLA

The modified OR-gate using multiplexer is placed in order to obtain minimum reduction in power consumption (W), area and delay (ns) .The inputs of modified OR-gate using multiplexer are 'a' ,'b' and the obtained output is 'y'.The obtained RTL schematic for modified OR-gate using multiplexer is shown in Fig.10, and the obtained RTL schematics for 16-bit and 32-bit for modified CSLA dominated by carry generation logic is shown in Fig.11, and Fig.12 and for 16-bit and 32-bit SQRT CSLA is shown in Fig.13, and Fig.14.

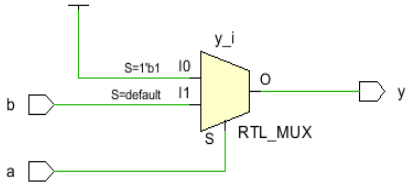


Fig.10: RTL schematic for modified OR-gate using multiplexer

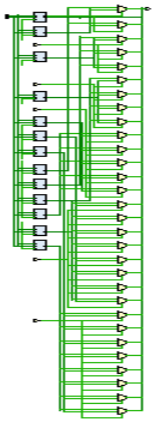


Fig.11: RTL schematicfor 16-bitmodified CSLA dominated by carry generation logic

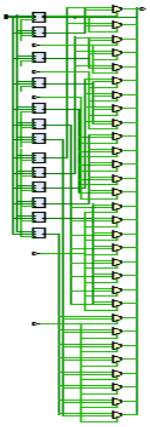


Fig.12: RTL schematicfor 32-bitmodified CSLA dominated by carry generation logic

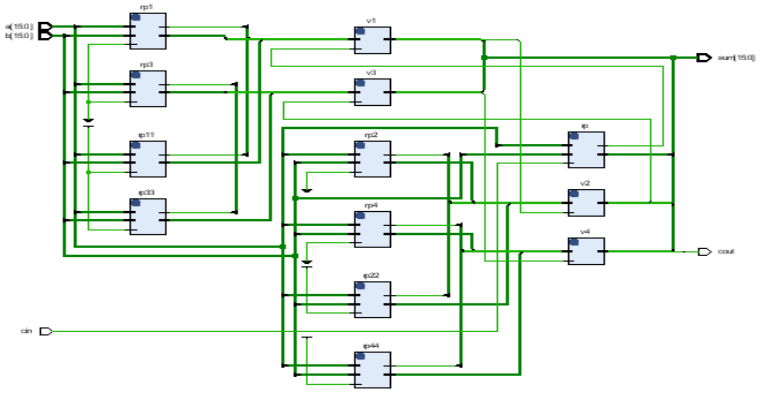


Fig.13: RTL schematic for 16-bit SQRT CSLA

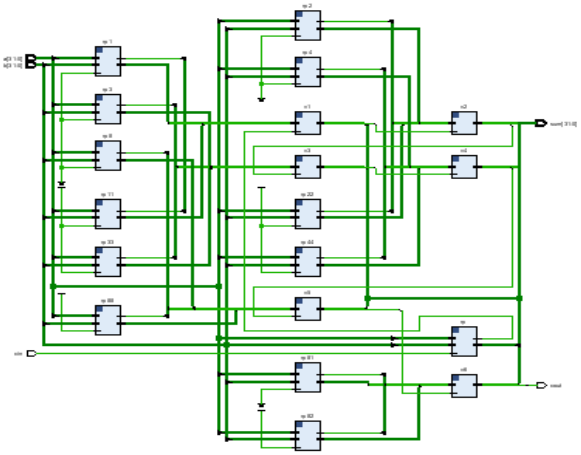


Fig.14: RTL schematic for 32-bit SQRT CSLA

The power consumption (W)andLUT's obtained for 16-bit and 32-bit for modified CSLA dominated carry generation logic is shown in Fig.15, Fig.16, and 16-bit and 32-bit for SQRT CSLA is shown in Fig.17, and Fig.18.Combinational delay for 16-bit and 32-bitfor modified CSLA dominated by carry generation logic is shown in Fig.19, and Fig.20, and 16-bit and 32-bit for SQRT CSLA is shown in Fig.21, and Fig.22.

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start
synth_1	constrs_1	synth_design Complete!								14	0	0.00	0	0	11/9/20 9:18
impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	9.273	0	14	0	0.00	0	0	11/9/20 9:25

Fig.15: LUT's and power for 16-bitmodified CSLA dominated by carry generation logic

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start
synth_1	constrs_1	synth_design Complete!								30	0	0.00	0	0	11/9/20 10:01 PM
impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	19.782	0	30	0	0.00	0	0	11/9/20 10:08 PM

Fig.16: LUT's and power for 32-bitmodified CSLA dominated by carry generation logic

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start
synth_1	constrs_1	synth_design Complete!								34	0	0.00	0	0	8/3/20 12:28 I
impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	11.817	0	32	0	0.00	0	0	8/3/20 12:29 I

Fig.17: LUT's and power for 16-bit SQRT CSLA

International Journal of All Research Education and Scientific Methods (IJARESM), ISSN: 2455-6211
Volume 8, Issue 12, December-2020, Impact Factor: 7.429, Available online at: www.ijaresm.com

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start
synth_1	constrs_1	synth_design Complete!								76	0	0.00	0	0	8/3/20
impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	24.523	0	76	0	0.00	0	0	8/3/20

Fig.18: LUT's and power for 32-bit SQRT CSLA

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement
Unconstrained Paths (1)											
(none) (10)											
Path 11	∞	4	3	a[1]	s[3]	7.162	3.516	3.646	49.1	50.9	∞
Path 12	∞	4	4	a[7]	s[10]	7.148	3.383	3.765	47.3	52.7	∞
Path 13	∞	4	2	a[13]	s[14]	7.110	3.517	3.593	49.5	50.5	∞
Path 14	∞	4	2	a[13]	s[15]	6.905	3.412	3.493	49.4	50.6	∞
Path 15	∞	3	2	a[5]	s[5]	6.762	3.486	3.276	51.6	48.4	∞
Path 16	∞	3	4	a[7]	s[8]	6.681	3.479	3.202	52.1	47.9	∞
Path 17	∞	3	3	a[1]	s[1]	6.604	3.372	3.232	51.1	48.9	∞
Path 18	∞	3	4	a[11]	s[11]	6.598	3.489	3.109	52.9	47.1	∞
Path 19	∞	3	3	a[1]	s[2]	6.589	3.359	3.230	51.0	49.0	∞
Path 20	∞	3	4	a[7]	s[7]	6.540	3.358	3.182	51.3	48.7	∞

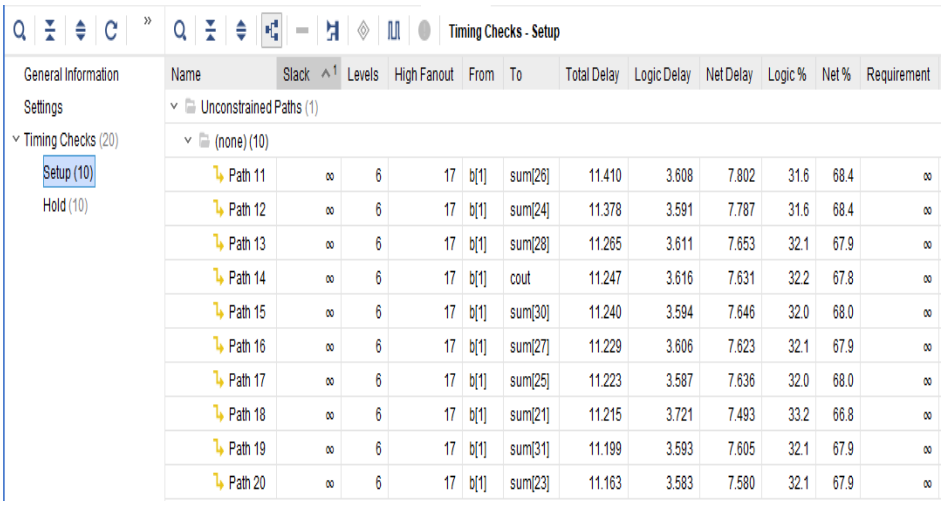
Fig.19: Combinational delay for 16-bitmodified CSLA dominated by carry generation logic

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement	Source Clock
Unconstrained Paths (1)												
(none) (10)												
Path 11	∞	5	3	a[17]	s[22]	9.424	3.699	5.725	39.2	60.8	∞	input port clock
Path 12	∞	5	3	a[17]	s[23]	9.393	3.595	5.797	38.3	61.7	∞	input port clock
Path 13	∞	5	3	a[25]	s[30]	9.196	3.625	5.571	39.4	60.6	∞	input port clock
Path 14	∞	5	3	a[25]	s[31]	9.090	3.460	5.630	38.1	61.9	∞	input port clock
Path 15	∞	5	3	a[17]	s[21]	8.857	3.568	5.289	40.3	59.7	∞	input port clock
Path 16	∞	4	4	a[0]	s[3]	8.797	3.495	5.302	39.7	60.3	∞	input port clock
Path 17	∞	4	3	a[8]	s[10]	8.785	3.363	5.422	38.3	61.7	∞	input port clock
Path 18	∞	4	4	a[11]	s[14]	8.769	3.502	5.267	39.9	60.1	∞	input port clock
Path 19	∞	4	3	a[25]	s[28]	8.733	3.538	5.194	40.5	59.5	∞	input port clock
Path 20	∞	5	3	a[25]	s[29]	8.627	3.493	5.134	40.5	59.5	∞	input port clock

Fig.20: Combinational delay for 32-bit modified CSLA dominated by carry generation logic

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement
Unconstrained Paths (1)											
(none) (10)											
Path 11	∞	5	10	a[3]	sum[10]	8.592	3.698	4.894	43.0	57.0	∞
Path 12	∞	5	10	a[3]	cout	8.518	3.495	5.023	41.0	59.0	∞
Path 13	∞	5	10	a[3]	sum[13]	8.382	3.550	4.833	42.3	57.7	∞
Path 14	∞	5	4	a[1]	sum[6]	8.218	3.605	4.613	43.9	56.1	∞
Path 15	∞	5	10	a[3]	sum[8]	8.166	3.680	4.486	45.1	54.9	∞
Path 16	∞	5	10	a[3]	sum[15]	8.110	3.573	4.537	44.1	55.9	∞
Path 17	∞	5	4	a[1]	sum[4]	8.109	3.699	4.410	45.6	54.4	∞
Path 18	∞	5	10	a[3]	sum[14]	8.107	3.575	4.531	44.1	55.9	∞
Path 19	∞	5	10	a[3]	sum[7]	8.064	3.563	4.501	44.2	55.8	∞
Path 20	∞	5	10	a[3]	sum[11]	8.030	3.575	4.455	44.5	55.5	∞

Fig.21: Combinational delay for 16-bit SQRT CSLA



Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %	Requirement
Unconstrained Paths (1)											
(none) (10)											
Path 11	∞	6	17	b[1]	sum[26]	11.410	3.608	7.802	31.6	68.4	∞
Path 12	∞	6	17	b[1]	sum[24]	11.378	3.591	7.787	31.6	68.4	∞
Path 13	∞	6	17	b[1]	sum[28]	11.265	3.611	7.653	32.1	67.9	∞
Path 14	∞	6	17	b[1]	cout	11.247	3.616	7.631	32.2	67.8	∞
Path 15	∞	6	17	b[1]	sum[30]	11.240	3.594	7.646	32.0	68.0	∞
Path 16	∞	6	17	b[1]	sum[27]	11.229	3.606	7.623	32.1	67.9	∞
Path 17	∞	6	17	b[1]	sum[25]	11.223	3.587	7.636	32.0	68.0	∞
Path 18	∞	6	17	b[1]	sum[21]	11.215	3.721	7.493	33.2	66.8	∞
Path 19	∞	6	17	b[1]	sum[31]	11.199	3.593	7.605	32.1	67.9	∞
Path 20	∞	6	17	b[1]	sum[23]	11.163	3.583	7.580	32.1	67.9	∞

Fig.22: Combinational delay for 32-bit SQRT CSLA

Table 1: Lut's, Delay And Power For 16-Bit Modified Csla Dominated By Carry Generation Logic Adder And Sqrt Csla Adder

S.NO	DIFFERENT ADDERS	LUT'S	DELAY(ns)	POWER(W)
1.	Regular SQRT CSLA adder	34	8.592	11.817
2.	ModifiedCSLA dominated by carry generation logic adder	14	7.162	9.273

Table 2: Lut's, Delay And Power For 32-Bit Modified Csla Dominated By Carry Generation Logic Adder And Sqrt Csla Adder

S.NO	DIFFERENT ADDERS	LUT'S	DELAY(ns)	POWER(W)
1.	Regular SQRT CSLA adder	76	11.410	24.523
2.	Modified CSLA dominated by carry generation logic adder	30	9.424	19.782

The combinational delay, power consumption and LUT's of 16-bit modified CSLA dominated by carry generation and SQRT CSLA is tabulated in TABLE 1, and similarly, the combinational delay, power and LUT's of 32-bit modifiedCSLA dominated by carry generation and SQRT CSLA istabulated in TABLE 2. When comparing to 32- bit modified CSLA dominated by carry generation adder and SQRT CSLA adder, the combinational delay, power consumption and LUT's are gradually reducing is tabulated in TABLE 1.

CONCLUSION

The modified CSLA dominated by carry generation logic and SQRT CSLA adder are coded in Verilog HDL andsimulation and synthesis results are carried out using Xilinx Vivado v2017.3 software tool. From the obtained results, it is observed that the LUT's, speed (ns) and power consumption (W) are reduced for modified CSLA dominated by carry generation logic. It is also observed that the LUT's are reduced by 60.52%, speed (ns) is improved by 17.40%, power consumption(W) is reduced by 19.33%for modified CSLA dominated by carry generation logic adder when compared to SQRT CSLA.

REFERENCES

[1] Minho Nam, Yeonhun Choi, Kyoungrok Cho, High-speed and energy efficient carry select adder (CSLA) dominated by carry generation logic, in Microelectronics Journal, Volume 79, September 2018, Pages 70-78.

[2] B. Ramkumar and Harish M Kittur, Low-Power and Area-Efficient Carry Select Adder, in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 2, FEBRUARY 2012, pages 371-375.
[3] D.K. Pradhan, Fault-tolerant carry-save adders, IEEE Trans. Comput. 100 (12) (1974) 1320–1322.
[4] R. Datta, J.A. Abraham, R. Montoye, W. Belluomini, H. Ngo, C. McDowell, et al., A low latency and low power dynamic carry save adder, in: Proc IEEE International Symposium on Circuits and Systems (ISCAS), vol. 2, 2004, pp. II477–II480.
[5] R. Mahalakshmi, T. Sasilatha, A power efficient carry save adder and modified carry save adder using cmos technology, in: Proc IEEE International Conference on Computational Intelligence and Computing Research (ICCIC), 2013.
[6] R.A. Javali, R.J. Nayak, A.M. Mhetar, M.C. Lakkannavar, Design of high speed carry save adder using carry lookahead adder, in: Proc IEEE International Conference on Circuits, Communication, Control and Computing (I4C), 2014, pp. 33–36.
[7] F.C. Cheng, S.H. Unger, M. Theobald, W.C. Cho, Delay-insensitive carry-lookahead adders, in: Proc IEEE International Conference on VLSI Design, 1997, pp. 322–328.
[8] Y.T. Pai, Y.K. Chen, The fastest carry lookahead adder, in: Proc Second IEEE International Workshop on Electronic Design, Test and Applications (DELTA), 2004, pp. 434–436.
[9] P. Celinski, J.F. Lopez, S. Al-Sarawi, D. Abbott, Low depth, low power carry lookahead adders using threshold logic, Microelectron. J. 33 (12) (2002) 1071–1077.
[10] M. Alioto, G. Palumbo, A simple strategy for optimized design of one-level carry-skip adders, IEEE Trans. Circ. Syst. I: Fund. Theor. Appl. 50 (1) (2003) 141–148.